REMARKS

Applicants respectfully request reconsideration and allowance of the subject application. Claims 1 and 29 are amended. Claims 1-33 are pending.

Rejection of Claims 1 and 29 under 35 U.S.C. § 112

In paragraph 2 of the Office Action, the Examiner rejected Claims 1 and 29 under § 112, *second paragraph,* as failing to particularly point out and distinctly claim that which Applicants regard as the invention.

In response to the Section 112, second paragraph rejection, Applicants have amended Claims 1 and 29 as indicated in the "MARKED UP VERSION OF PENDING CLAIMS" (attached hereto) to remove the basis for the rejection of such Claims. In light of the aforementioned amendment, Applicants respectfully assert that Claims 1 and 29 are now in condition for allowance and respectfully requests that the Section 112, second paragraph rejection of such claims be withdrawn.

Rejection of Claims under 35 U.S.C. § 103

In paragraph 4 of the Office Action, the Examiner rejected claims 1-5, 12, 14-19, 22, 29, 31-33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,689,688 to Strong et al. (hereinafter, "Strong") in view of U.S. Patent No. 5,860,096 to Undy et al. (hereinafter, "Undy"). Applicants respectfully traverse the rejection.

Strong is directed to synchronizing internal times maintained by network nodes to a reference time source. (Col. 1, lines 10-13). Strong uses a master node

to synchronize times for slave nodes by using a synchronization message bearing a reference time stamp according to a time scale maintained by the master node. (Col. 9, lines 31-41). Thus, Strong is primarily concerned with techniques for calculating and improving the "accuracy of synchronization." (Col. 18, lines 53-57). Considerable time is spent teaching how to calculate synchronization times accurately. For example, Col. 10, lines 35-68 show equations used to calculate the synchronization time.

Undy is directed to the amount of "on-chip space" needed for "an instruction cache system." (Col. 1, lines 40-42). Undy teaches that the cache can be separated into a "small cache" dedicated to instructions and a "larger cache" used for both instructions and data. A "prefetch buffer" is used to transfer instructions from the larger cache to the smaller cache with minimal delay. (Col 1, lines 48-58). Undy is concerned with providing an "instruction cache" for a processor that is "fast" and "is relatively small so that it may be placed internal to an integrated circuit processor." (Col. 4, lines 40-43)

The Examiner cites the combination of Strong and Undy in the § 103 rejection of all the independent Claims (e.g., Claims 1, 15, 23, and 29). Independent Claims 1, 15, 23, and 29 of Applicants' application, each recite language that defines various ways for synchronizing data among a plurality of web servers. For example, Claim 1 recites:

> 1. (Once Amended) A method for synchronizing data among a plurality of web servers each of the plurality of web servers is coupled to a common data server, the method comprising:
>
> retrieving a scheduled activation time from the data server;
>
> prior to the scheduled activation time, retrieving updated data into staging caches in the plurality of web servers; and

at the scheduled activation time, copying the updated data from the staging caches within each of the plurality of web servers to an active cache within each of the plurality of web servers, respectively.

The cited references do not teach or suggest this method. In fact, neither Strong nor Undy appear to have much relevance to Applicants' Claims.

Neither reference teaches, for example, (i) "maintaining data synchronization among a plurality of web servers using a common data server," (ii) "retrieving a scheduled activation time from the data server" (iii) "retrieving updated data into staging caches in the plurality of web servers;" or (iv) "at the scheduled activation time, copying the updated data from the staging caches within each of the plurality of web servers to an active cache within each of the plurality of web servers, respectively." (See, e.g., Claim 1).

Again, Strong teaches techniques for synchronizing local times maintained by the nodes within a network. (See, i.e., Abstract, Lines 1-3). Nowhere is Strong remotely concerned with data synchronization techniques as claimed by using "staging caches" and "active caches" in conjunction with a "scheduled activation time" as recited in Claim 1.

Similarly, Undy is merely concerned with providing "a two level instruction cache for providing fast instruction access much of the time using minimal penalty for an instruction cache miss." (See Undy, Col. 4, lines 39-43). Again, Undy is concerned with cache size and speed on a chip; not "data synchronization" among a plurality of web servers as recited in Applicants' independent Claims.

Furthermore, the combination of Strong and Undy also fail to teach using "a staging cache," "active cache" and "a scheduled activation time" to synchronize data among a "plurality of web servers." Strong and Undy are entirely silent as to these features in Claim 1 as well as the other independent claims.

In paragraph 4 of the Office Action, the Examiner argues that "Strong discloses a method of synchronization among a plurality of nodes (web servers) in a network wherein each node is coupled to a common master node (data server)." Applicants respectfully disagree with the Examiner's generalization that Strong's use of the word "synchronization" has anything to do with the type of data synchronization recited in Applicants' claims.

The "synchronization" Strong is referring to is the "synchronization of times" maintained at the plurality of nodes. (See i.e., line 1-3 of the Strong Abstract). Applicants' independent Claims, on the other hand, use the term "synchronization" in the context of "synchronizing data" among a plurality of "web servers," not the "synchronizing of local times maintained at nodes" as taught by Strong.

The Examiner appears to go on to argue that the "synchronization message" described in Strong is the same as the "scheduled activation time" recited in the independent Claims. Applicants respectfully disagrees with this argument, because the "synchronization message" described in Strong has to do with clock synchronization at a node (see, i.e., Abstract) and does not remotely teach or suggest using the message for purposes of indicating a time for copying data from a "staging cache" to an "active cache" at the "scheduled activation time" as recited in Applicants' Claims.

The Examiner admits that "Strong fails to explicitly disclose "[r]etrieving updated data into the staging caches in the plurality of web servers; "[c]opying data from the staging cache of each web server to an active cache of each web server." For these features, however, the Examiner (on page 3 of the Office Action) argues that Undy discloses a system for synchronizing a network including "retrieving updated data into the staging cache (larger cache) (col. 1, lines 20-22, 45-48, col. 2 lines 10-13, col. 5 lines 19-20)" and "[c]opying data from the staging cache (larger cache) to an active cache (smaller cache) (col. 3, lines 5-7, col. 7, lines 1-2, col. 5, lines 1-4).

The Applicants' are, respectfully, unable to find any basis to support the Examiner's interpretation of the alleged teachings of Undy.

Again, Undy is concerned with cache memory system architectures used in conjunction with processors and chip size (see, i.e., Col 4, lines 39-43). There is no discussion that remotely teaches or suggests anything close to a system for synchronizing data among a plurality of web servers as recited in Applicants' Claims.

Furthermore, Undy is devoid of anything that remotely teaches or suggests synchronizing data among "web servers" by using a "staging cache," "active cache" and a "scheduled activation time." The "large" and "small" cache described in Undy and referenced by the Examiner for support of her argument, in fact, has nothing to do with synchronizing data among a "plurality of web servers" as recited in Applicants' claims. Rather the "large" and "small" caches in Undy are used for storing instructions needed by a processor and are separated into "large" and "small" caches for the purpose of speeding up access to the instructions by the processor and for reducing chip size. (See, i.e., Undy Col. 2,

lines 26-41 and Col. 4, lines 39-43). Undy's "large" and "small" caches have absolutely nothing in common with a "staging cache" and an "active cache" used for purposes of synchronizing data among a plurality of web servers as recited in Applicants' Claims. Again, Undy is concerned with chip space and access speed of instructions to the processor, whereas Applicants' Claims are directed to web servers and using a "staging cache" and an "active cache" for synchronizing data among the servers.

Accordingly, Applicants respectfully believe that the two primary references cited by the Examiner (Strongy and Undy) as the basis for rejecting all independent Claims were not properly interpreted and do not remotely teach or suggest what the Examiner alleges they teach.

Because neither Stong and/nor Undy teach or suggest what the Examiner purports they teach or suggest, it is not possible to combine Strong and Undy to arrive at Applicants' claimed invention. Additionally, it is not possible to combine any of the other references cited by the Examiner with Strong and Undy to arrive at the solutions claimed by the Applicants, because of the failure of Strong and/or Undy to teach or suggest what the Examiner purports they teach or suggest. Accordingly, none of the references cited in the Office Action, teach, suggest or provide any motivation to arrive at the solutions claimed by the Applicants.

Therefore, based on all of the above comments, the Examiner has failed to establish a *primae facie* case of obviousness with respect to independent Claims 1, 15, 23, and 29 and any claims dependent thereon. For these reasons alone, Applicants respectfully request that the § 103 rejection of all the claims be withdrawn.

Conclusion

The Applicants respectfully request the rejections be withdrawn and solicits a Notice of Allowance for Claims 1-33. If any issues remain that prevent issuance of this Application, the Examiner is urged to contact the undersigned attorney before issuing a subsequent Action.

Respectfully Submitted,

Date: 10/21/02

By: _____

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MARKED UP VERSION OF PENDING CLAIMS UNDER 37 C.F.R. 1.121(C)(1)(ii):

Please amend claim 1 and 29 as follows and in accordance with 37 C.F.R. 1.121(c)(1)(ii), by which the Applicants submit the following marked up version only for claims being changed by the current amendment, wherein the markings are shown by brackets (for deleted matter) and/or underlining (for added matter):

1. (Once Amended) A method of synchronizing data among a plurality of web servers, wherein each of the plurality of web servers is coupled to a common data server, the method comprising:

retrieving a scheduled activation time from the data server;

prior to the scheduled activation time, retrieving updated data into staging caches in the plurality of web servers; and

at the scheduled activation time, copying the updated data from the staging caches in each of the plurality of [each] web servers to an active cache within each of the plurality of web servers, respectively.

29. (Once Amended) A method of synchronizing data among a plurality of web servers, wherein each of the plurality of web servers is coupled to a common data server, the method comprising:

providing a scheduled activation time from the data server to each of the plurality of web servers;

communicating updated data into a staging cache in each of the plurality of web servers prior to the scheduled activation time; and

copying data from the staging cache [of] in each of the plurality of web servers to an active cache in each of the plurality of the web servers, respectively, at the scheduled activation time.